50G PAM4 Technical White Paper

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01 Technical Background

1.1 PAM4 Overview

PAM4 is a branch of the pulse amplitude modulation (PAM) technology, which is a mainstream signal transmission technology following non-return-to-zero (NRZ). Playing a key role in multi-order modulation, PAM is widely used in high-speed signal interconnection. Figure 1-1 shows the typical waveform of NRZ and 4-order PAM (PAM4) signals. The right part of this figure compares the eye diagrams of NRZ and PAM4 signals, where an NRZ signal uses the single-pupil waveform and a PAM4 signal uses three-pupil wavelength (three eye diagrams along the y axis).

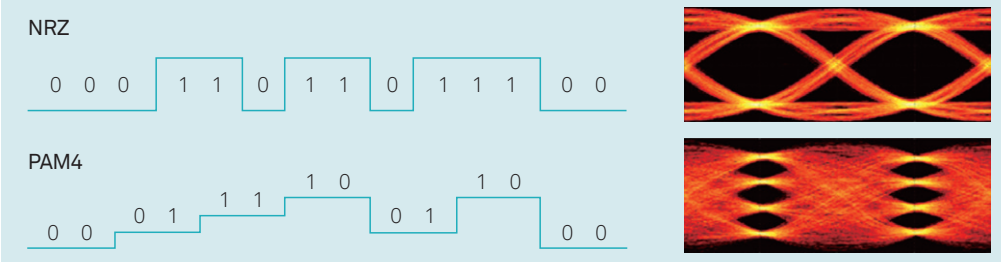


Figure 1-1 Comparison of waveforms and eye diagrams between NRZ and PAM4 signals

The differences between NRZ and PAM4 signals are as follows:

- An NRZ signal uses high and low signal levels to represent 1 and 0 in digital logic signals. Within each clock period, one bit of logic information can be transmitted.
- A PAM4 signal uses four signal levels for transmission. Within each clock period, two bits of logic information, that is, 00, 01, 11, and 10, can be transmitted.

Therefore, under the same baud rate, the bit rate of a PAM4 signal is twice that of an NRZ signal, doubling transmission efficiency and reducing transmission costs. With its high efficiency, 50 Gbps/lane (50G for short) PAM4 has been chosen by IEEE 802.3 as the encoding technology at the physical layer for 400GE, 200GE, and 50GE interfaces.

1.2 Background

PAM4 is an efficient modulation technology that improves bandwidth utilization.

1.2.1 High-Bandwidth and Cost-Effective Solution Required by 5G Transport Networks

Cost cutting

The transition from 4G to 5G is accompanied by a sharp increase in data traffic. In contrast, carriers' revenue is growing slowly, widening the scissors. Balancing data traffic and income is a pain point of carriers but also an opportunity for those who can resolve the pain point to get competitive edges in 5G solutions. Cutting costs is the best way to narrow the scissors. In the cost structure of devices on a mobile network, optical modules account for an ever-increasing percentage. Decreasing the costs of optical modules is critical in cutting the overall costs.

Performance improvement

5G mobile networks will surely outperform previous generations of mobile networks in performance. For example, a 5G network provides a peak downlink data rate of 20 Gbit/s and a peak uplink data rate of over 10 Gbit/s. Regarding 5G infrastructure, carriers should reconstruct the network architecture on an end-to-end basis so as to build an elastic architecture covering the access network, aggregation network, and core network, which enhances the flexibility in bandwidth expansion.

Building on the 50G PAM4 per lane technology, 400GE/200GE/50GE interfaces can meet the cost and performance requirements of 5G mobile networks to construct an optimal solution covering the access network, aggregation network, and core network.

1.2.2 Electric Technology Needed to Boost Optical Technology Development and Eliminate Bottlenecks of High-Capacity Access Technologies

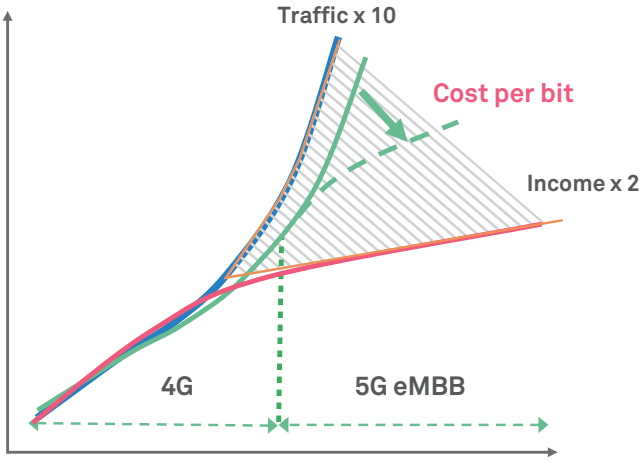


Figure 1-2 Scissors of carriers' income and data traffic

The optoelectronic technology is a branch of the semiconductor technology. Compounds of III-V group elements are commonly used in optical chip design to improve luminous efficiency and performance. This design is different from the complementary metal-oxide-semiconductor (CMOS) technology that uses pure silica to ensure the electrical performance.

The optical technology development has been a bottleneck of interface development. CMOS is a mature technology that has been widely adopted and optimized through N iterations through decades of development. In contrast, the III-V group falls far behind in terms of technical maturity and standardization due to a limited industry scale. The development of the optical technology does not meet Moore's law (performance will double every 18 months). The performance of optoelectronic chips doubles every 24 to 36 months in the communications field.

The silicon photonics technology and higher-order modulation arise to promote optoelectronic technology development. PAM4 is a type of higher-order modulation technology which effectively accelerates optical technology development using the electric technology.

02 Standards Progress

2.1 Progress of PAM4-related Standards

The Ethernet technology has been using the NRZ modulation code ever since it appeared in 1980s. Only 100BASE-T interfaces use the multi-order modulation code. After developing to 100GE, the Ethernet technology encounters a bottleneck in bandwidth improvement due to cost reduction challenges facing physical layer technologies.

When discussing the modulation solution for the 400GE (802.3bs) standard, some vendors proposed replacing NRZ with PAM4 as the modulation code at the physical layer.

This proposal was accepted after thorough discussion, technical analysis, and argumentation. 400GBASE-LR8/FR8 is the first standard that applies PAM4 at the optical layer. Later, IEEE used the PAM4 code in the 200GE/50GE standards.

Currently, the 400GE, 200GE, and 50GE standards all use the PAM4 modulation technology with the baud rate of 26.5625 GBd (The corresponding bit rate is 53 Gbps due to PAM4 modulation. The bit rate of 50 Gbps is used in this document for convenience).

2.2 Progress of 400GE/200GE Standards

The IEEE 802.3bs standard baseline was completed in early 2015, and the standard was completed in December 2017.

802.3bs covers two Ethernet interface rates: 400GE and 200GE. The 400GE standard defines various AUI electrical interfaces and specifications of PMD sublayers, such as LR8 (10 km), FR8 (2 km), DR4 (500 m), and SR16 (100 m). Among Ethernet standards, LR8 and FR8 are the first to use the 50G PAM4 technology, which paves the way for the wide commercial application of PAM4. Here, digit 8 indicates 8 lanes. Each lane provides the bit rate of 50 Gbps and these lanes form as a 400GE interface.

The 400GE/200GE 40 km standard was also discussed in the IEEE 802.3 Beyond 10 km workgroup. In March 2018, the 200GE 40 km standard passed the objective review, which means this standard is only one step away from project initiation.

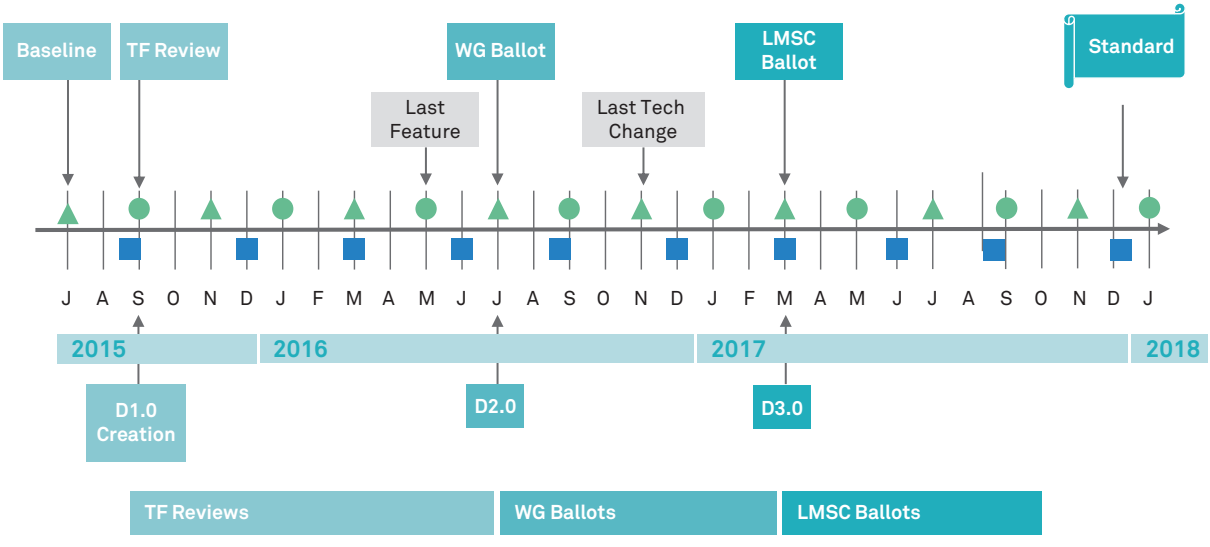


Figure 2-1 Timeline of 400GE/200GE standards

2.3 Progress of the 50GE Standard

The IEEE 802.3cd standard baseline was completed in September 2016 and Draft 3.2 has been completed now, two months ahead of the schedule. The standard is planned to be released in September 2018.

802.3cd is still under formulation but has attracted extensive attention in the industry because the market for 50GE interfaces has emerged. Driven by the high anticipation for 50GE in the industry, the preparation of the 50GE standard is faster than that of the 400GE/200GE standards. The 50GE standard covers sublayers including 50GBASE-LR, KR, and SR PMD. All PMD sublayers adopt the 50G PAM4 technology. 50GE is the most widely used Ethernet interface rate in the PAM4 technology.

The 50GE 40 km standard was also discussed in the IEEE 802.3 Beyond 10 km workgroup. In January 2018, this standard passed the objective review almost unanimously. It is highly recognized in the industry.

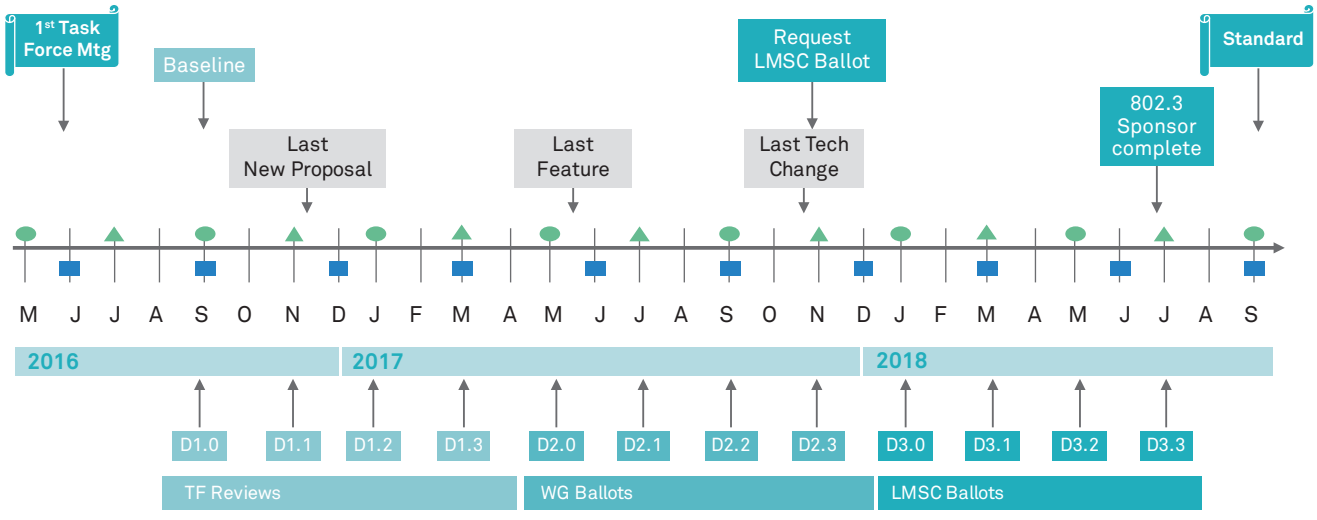


Figure 2-2 Timeline of the 50GE standard

03 Key Technologies

3.1 Overview

50G PAM4-based 400GE/200GE/50GE face a plurality of challenges in developing key technologies. In IEEE standard activities, these challenges have been resolved through joint efforts of mainstream vendors in the industry.

The application of 50G PAM4 based on the IEEE standard framework is secure and reliable and allows multi-vendor interoperability.

3.2 400GE/200GE/50GE Technologies

IEEE 802.3 is a series of Ethernet technology standards that define the technical specifications of the first layer (physical layer) and second layer (data link layer) in the OSI model.

3.2.1 50GE Technology

IEEE officially launched the 50GE standard project in May 2016. The 50GE standard shares the same architecture as the 400GE/200GE standard. This section introduces the technologies of the 50GE PMD sublayers.

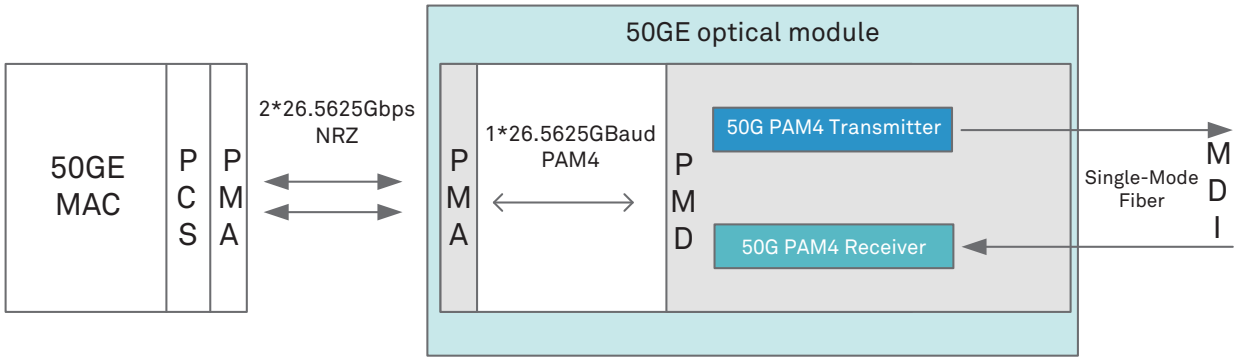


Figure 3-1 50GBASE-LR PMD architecture

Architecture description:

- The physical coding sublayer (PCS) is responsible for signal coding/encoding, scrambling/descrambling, alignment insertion/removal, and sorting and control. Especially, the PCS supports forward error correction (FEC).
- The physical medium attachment sublayer (PMA) is responsible for matching the PCS and PMD and supports various functions such as mapping, multiplexing/demultiplexing, and clock restoration. In addition, the PAM provides optional functions for diagnosis assistance, such as loopback and test pattern.
- The physical medium dependent sublayer (PMD) is responsible for the interfaces for physical transmission. One Ethernet rate may exist at multiple PMDs to match different physical interfaces at different transmission distances and media (such as electrical or optical). The PMD also supports detection on data channel signals.
- The medium dependent interface (MDI) is a type of physical medium, such as the optical fiber and cable.
- 50GE MAC uses the 50GAUI-2 interfaces (2 x 26.5625 Gbit/s) to transmit data to the 50GE optical module (QSFP28 encapsulation) through the PCS and PMA. During the transmission, the PMA aggregates two lanes into one and converts the modulation code to PAM4 with the baud rate of 26.5625 GBaud.
- Data is then transmitted to the PMD. The transmitter and receiver at the PMD implement electrical-optical conversion and optical-electrical conversion respectively.
- In the transmit direction, 50GE has only one lane. The transmitter performs electrical-optical conversion and sends signals to an optical fiber. That is, data is transmitted from the PMD to the MDI through a single-mode optical fiber.
- In the receive direction, optical fibers forward signals to the receiver for optical-electrical conversion. The converted signals are then sent to the PMA.

Key parameters of the transmitter, receiver, and power budget are listed as follows.

Parameter	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		–
Wavelengths (range)	1304.5 to 1317.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Average launch power (max)	3	4.2	dBm
Average launch power (min)	–4.1	–4.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	2.8	4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)	–2.5	–1.5	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–3.9	–2.9	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3.2	3.4	dB
Average launch power of OFF transmitter (max)	–16		dBm
Extinction ratio (min)	3.5		dB
RIN17.10MA (max)	–132	–	dB/Hz

Figure 3-2 Parameters of the 50GBASE-LR transmitter

Description of transmitter's key parameters:

» Signaling rate: 26.5625 GBaud. 50GBASE-LR uses a single lane and the rate after KP4 FEC encoding. The rate is consistent with those of 400GBASE-LR8 and 200GBASE-LR4.

» Average launch power: This parameter defines the maximum and minimum average optical power of a transmitter. This parameter is for reference only and is not used for power budget calculation.

» Outer optical modulation amplitude: This parameter defines the maximum and minimum optical modulation amplitude (OMA) optical power of a transmitter. IEEE attaches great importance to OMA optical power because it contains the extinction ratio (ER). ER can help determine whether the output optical power of a transmitter meets the requirements specified in the standard.

» Launch power in OMA minus TDECQ: This parameter is the minimum value of the launch power of the OMA optical module minus TDECQ.

» Transmitter and dispersion eye closure for PAM4 (TDECQ): PAM4 eye closure caused by transmitters and dispersion in each lane. This parameter measures whether the performance of a transmitter meets the basic requirements for transmitting PAM4 signals.

» Extinction ratio: This parameter is an important optical parameter of transmitters. The ER of NRZ signals is the ratio between the average optical power of signal 1 and signal 0, whereas the ER of PAM4 signals is the ratio between the average optical power of signal 3 and signal 0.

Description	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		–
Wavelengths (range)	1304.5 to 1317.5		nm
Damage threshold	5.2	5.2	dBm
Average receive power (max)	3	4.2	dBm
Average receive power (min)	–8.1	–10.8	dBm
Receive power (OMA_{outer}) (max)	2.8	4	dBm
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA_{outer}) (max)	Equation (139–1)	Equation (139–2)	dBm
Stressed receiver sensitivity (OMA_{outer}) (max)	–5.1	–6.4	dBm
Conditions of stressed receiver sensitivity test:			
Stressed eye closure for PAM4 (SECQ)	3.2	3.4	dB

Figure 3-3 Parameters of the 50GBASE-LR receiver

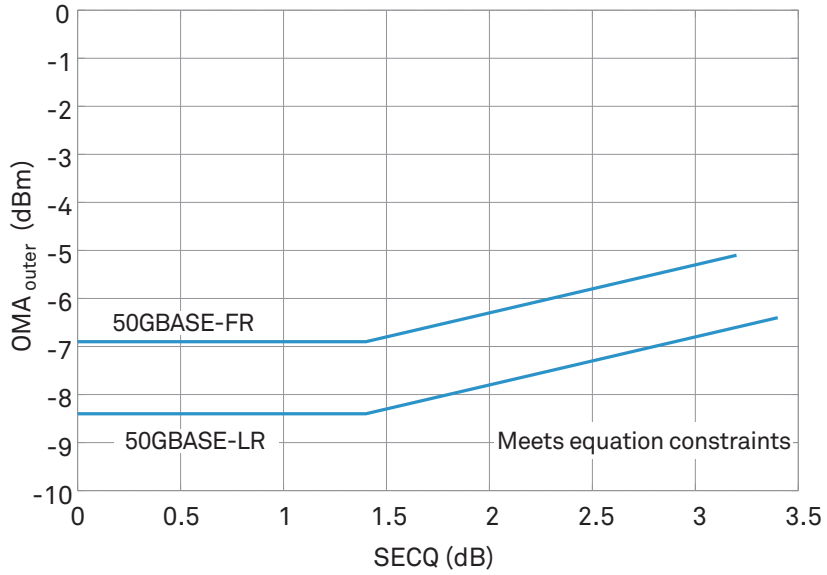


Figure 3-4 50GBASE-LR SECQ specifications

Description of the receiver's key parameters:

» Signaling rate: 26.5625 GBaud. This is the symbol transmit rate

» Average launch power: This parameter defines the maximum and minimum average optical power of a receiver. This parameter is for reference only and is not used for power budget calculation.

» Receive power OMA: This parameter defines the maximum and minimum OMA optical power of a receiver.

» Receiver sensitivity OMA: This parameter defines the OMA sensitivity of a receiver. Since this standard is being formulated, you can refer to the above parameter diagram or the following formula for the value of this parameter. The maximum value of this parameter varies with the value of stressed eye closure for PAM4 (SECQ for short).

RS = max(-6.9, SECQ-8.3) (dB)
RS = max(-8.4, SECQ-9.8) (dB)

» Stressed receiver sensitivity OMA: This parameter defines the stressed sensitivity specifications.

Parameter	50GBASE-FR	50GBASE-LR	Unit
Power budget (for maximum TDECQ)	7.6	10.3	dB
Operating distance	2	10	km
Channel insertion loss	4	6.3	dB
Maximum discrete reflectance	See 139.10.2.2	See 139.10.2.2	dB
Allocation for penaltiesc (for maximum TDECQ)	3.6	4	dB
Additional insertion loss allowed	0	0	dB

Figure 3-5 50GBASE-LR power budget specifications

Description of power budget parameters:

- Power budget (for maximum TDECQ): This parameter defines the theoretical power budget. The value of this parameter is the sum of lane insertion loss, allocation for penalties (for maximum TDECQ), and additional insertion loss allowed. It is a theoretical value and does not need to meet requirements.
- Channel insertion loss: This parameter defines the insertion loss brought by optical fibers and fiber connectors. According to IEEE, in a 50G LR scenario, the lane insertion loss is 1304.5 nm under extreme conditions. Given 0.43 dB/km, the total attenuation is 4.3 dB (0.43 db/km x 10 km). A margin of 2 dB (6.3 db – 4.3 dB) is reserved for the insertion loss caused by fiber connections and fiber fusion, which is consistent with the margin in 100GE.
- Receive power OMA: This parameter defines the maximum and minimum OMA optical power of a receiver.
- Allocation for penalties (for maximum TDECQ): This parameter defines the penalties for the maximum TDECQ. This parameter is for reference only and does not need to be tested or calculated.
- Additional insertion loss allowed: No margin needs to be reserved for the insertion loss in 50GE/200GE/400GE.
- Calculation of power budget: The calculation of power budget for 50GE is adjusted. The minimum requirements are as follows:
  Minimum value of Outer optical modulation amplitude – OMA sensitivity ≥ Channel insertion loss, that is, –1.5 dBm – (–8.4 dBm) = 6.9 dBm > 6.3 dBm
  As the replacement of TDECQ, SECQ is included in the sensitivity specifications of receivers. The sensitivity specifications of receivers contain specifications under the SECQ condition (equivalent to penalties for TDECQ). Therefore, penalties for TDECQ of transmitters do not need to be considered.

The following table describes 50GE 40km power budget forecast:

Parameter	50GBASE-LR	50GBASE-ER (Forecast)	Unit	Analysis
Power Budget	10.3	20	dB	This parameter is for reference only and does not need to be measured.
Operating distance	10	40	km	
Insertion loss	6.3	18	dB	Use the 100GE 40km specification, 0.4dB/km. Reserve 2dB for insertion losses of the fiber connector and splice fibers.
Outer Optical Modulation Amplitude (OMAouter)(min)	-1.5	4.5	dBm	This parameter is based on the mainstream EML capability in the industry.
Receiver sensitivity (OMAouter) (max)	-8.4 (SECQ < 1.4)	-13.5	dBm	This parameter is based on the mainstream 25G APD capability in the industry.
Allocation for penalties (for maximum TDECQ)	4	4	dB	Use EML for the 40km specification, which cannot be greater than that for the 10km specification.
Additional insertion loss allowed	0	0	dB	No optical power needs to be reserved for insertion losses.

The 50GE 40km standard was just initiated. The PAM4 modulation format will continue to be used, but key specifications are adjusted to meet the requirements for the 40km transmission distance. It is estimated that IEEE will continue using the 18dB insertion loss defined for 100GE. The difference between the minimum OAM transmit optical power and the OMA receiver sensitivity should be greater than or equal to 18 dB.

According to the preliminary analysis on the specifications of mainstream solutions in the industry, the transmit-side and receiver-side specifications are greatly improved compared with the 10km standard. It is estimated that the minimum OAM transmit optical power will be increased to +4.5 dBm and the OMA receiver sensitivity will be -13.5 dBm. This meets the 18 dB insertion loss requirement. Because IEEE needs to balance the benefits for every vendor, the specifications are not finally set yet.

3.2.2 400GE/200GE Technologies

Since 400GE/200GE technologies are similar to the 50GE technology, this section describes only the architecture of the technologies instead of providing details.

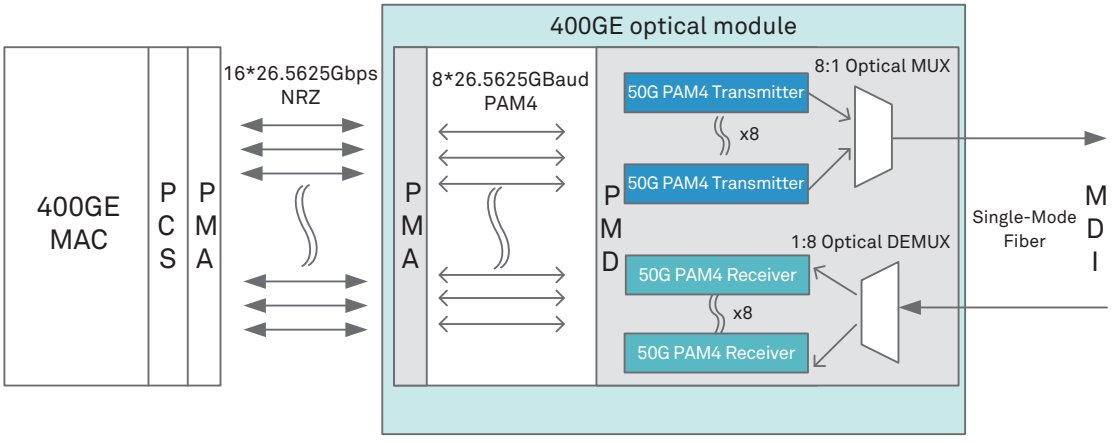


Figure 3-6 400GBASE-LR8 PMD architecture

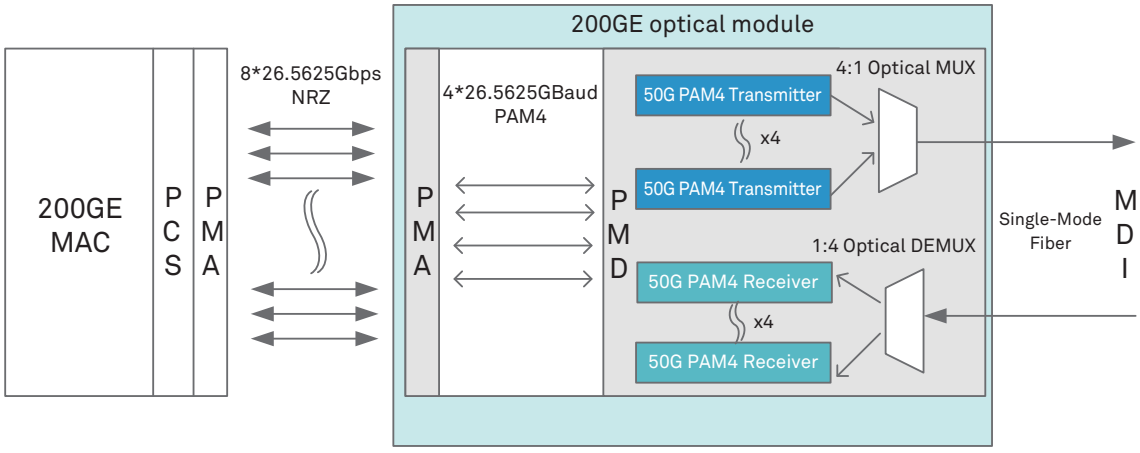


Figure 3-7 200GBASE-LR8 PMD architecture

Description of the 400GE architecture:

- 400GE MAC uses the 400GAUI-16 interfaces (16 x 26.5625 Gbit/s) to transmit data to the 400GE optical module (CFP8) through the PCS and PMA. During the transmission, the PMA aggregates 16 lanes into 8 lanes and converts the code to PAM4 with the baud rate of 26.5625 GBaud.
- Data is then transmitted to the PMD. The transmitter and receiver at the PMD implement electrical-optical conversion and optical-electrical conversion respectively.
- In the transmit direction, eight transmitters perform electrical-optical conversion, and each transmitter corresponds to one wavelength (see the wavelength specifications). Then signals from the eight lanes are multiplexed to one optical fiber. That is, data is transmitted from the PMD layer to the MDI layer through a single-mode optical fiber.
- In the receive direction, the optical fiber demultiplexes the eight wavelengths on the optical fiber to eight receivers for optical-electrical conversion. The converted signals are then sent to the PMA.

The 200GE architecture is almost the same as the 400GE architecture. The two differ in the number of lanes.

3.3 50G PAM4-based Optical Module Technologies

With the PAM4 encoding technology, the amount of information transmitted on 50G PAM4-based optical modules within each sampling cycle doubles. A 25G optical component can be used to achieve a 50 Gbit/s transmission rate, reducing the costs of optical modules.

50G PAM4 applies to multiple scenarios, such as single-lane 50GE PAM4 optical modules, 4-lane 200GE optical modules, and 8-lane 400GE optical modules.

3.3.1 Functions of Optical Modules

This section introduces the functions of a single-lane 50GE PAM4 optical module.

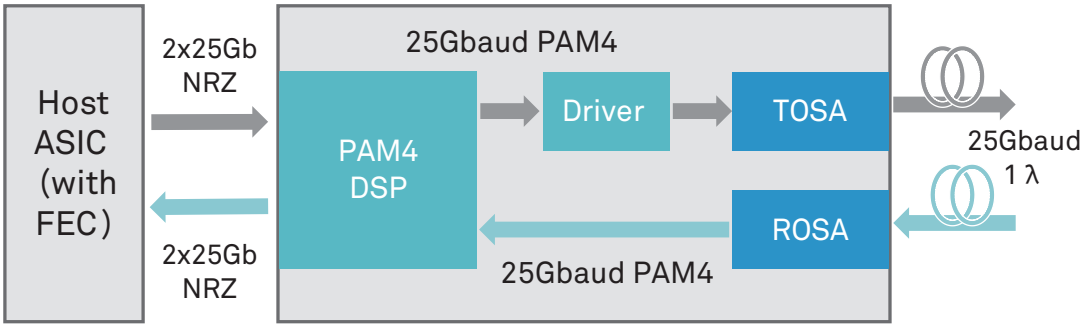


Figure 3-8 Working principle of a 50GE PAM4 optical module

The working principle of a 50GE PAM4 optical module is described as follows:

» In the transmit direction, the PAM4 encoding chip aggregates two 25 Gbit/s NRZ signals into one 25 GBaud PAM4 signal. The laser drive chip amplifies the PAM4 signal, and the 25 Gbit/s laser converts the electrical signal into a 25 GBaud (50 Gbps) single-wavelength optical signal.

» In the receive direction, the detector converts the 25 GBaud single-wavelength optical signal into an electric signal. The electric signal is shaped and amplified, and then output to the PAM4 decoding chip. The PAM4 decoding chip converts the signal into two 25 Gbit/s NRZ signals.

The 50GE PAM4 optical module uses the QSFP28 encapsulation mode, LC optical interfaces, and single-mode optical fibers. The transmission distance is 10/40 km, and the maximum power consumption is 4.5 W.

3.3.2 Specifications of Optical Modules

The performance of transmitters and receivers on optical interfaces of 50GE PAM4 optical modules must comply with the IEEE 802.3bs and IEEE 802.3cd standards.

An optical module provides N 25 Gbit/s electrical interfaces. For a 50GE optical module, the two electrical lanes transmit TX1/RX1 and TX2/RX2 signals specified in the SFF-8436_MSA standards. The performance of electrical interfaces must comply with the CEI-28G-VSR LAUI-2 standard.

The optical module with a transmission rate of 50 Gbit/s on a single wavelength supports 50GE, 200GE, and 400GE interfaces. The following table lists the parameters for the 50G, 200GE, and 400GE technical solutions.

Interface	Bandwidth	Electrical I/O	Optical I/O	Technology
50GBASE-LR/ER	50 Gbit/s	2 x 25 Gbit/s NRZ	1 x 50G PAM4	1 x 50 Gbit/s 1310 nm PAM4, 1λ
200GBASE-LR4	200 Gbit/s	8 x 25 Gbit/s NRZ	4 x 50G PAM4	4 x 50G PAM4 LAN-WDM, 4λ
400GBASE-LR8	400 Gbit/s	16 x 25 Gbit/s NRZ	8 x 50G PAM4	8 x 50G PAM4 LAN-WDM, 8λ

3.3.3 Technical Solution of PAM4 Optical Modules

I. Optical Component and Drive Chip

50G PAM4 optical modules use mature 25 Gbit/s optoelectronic chips to deliver cost-effective solutions. In 50GBASE-LR (10 km) scenarios, uncooled direct modulated laser (DML) transmitter optical subassemblies (TOSAs) with TO packaging are used. Such a solution features mature technologies, low costs, low power consumption, and easy mass production. The linear DML driver chip can convert input PAM4 voltage electric signals into current signals that can directly drive lasers. Such chips deliver a high bandwidth and output large drive current. Their maximum working rate can reach 28 GBaud. At the receive end, receiver optical subassemblies (ROSAs) with TO packaging are used. 25 Gbit/s pins and linear transimpedance amplifier (TIA) chips are integrated to the ROSAs.

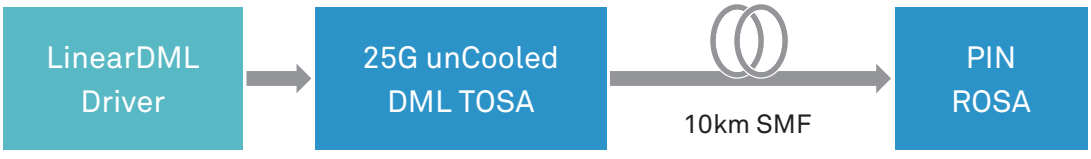


Figure 3-9 Optical components in 50GBASE-LR scenarios

In 50GBASE-ER (40 km) scenarios, 25 Gbit/s electro-absorption modulated laser (EML) TOSAs with BOX packaging are used. External cavity modulated distribution feedback (DFB) lasers, isolators, monitoring diodes, thermistors, and EML components are integrated to the TOSAs and driven by voltage signals. Such a solution features wide linear domains, high ER, high output optical power, and low TDECQ. Linear EML drive chips can amplify input PAM4 signals and output them to next EMLs. These chips provide a high bandwidth, a small jitter, an adjustable output gain, and a working rate up to 28 GBaud. At the receive end, APD ROSAs with TO packaging are used. 25 Gbit/s APDs and linear TIA chips are integrated into the ROSAs. Such ROSAs feature high sensitivity and apply to long-distance (40 km) transmission.

Figure 3-10 Optical components in 50GBASE-ER scenarios

II. PAM4 Chip

PAM4 codec chips perform conversion between NRZ signals and PAM4 signals inside modules. In the transmit direction, PAM4 chips shape, amplify, and convert two 25 Gbit/s NRZ signals output by boards into one 25 GBaud PAM4 signal. In the receive direction, PAM4 chips use the analog to digital converter (ADC) and digital signal processing (DSP) technology to decode the one 25 GBaud signal to two 25 Gbit/s NRZ signals.

III. Differences Between Solutions of NRZ and PAM4 Modules

The optical components and chips of PAM4 modules are very different from those of NRZ modules. The following table lists the differences between 50G QSFP28 LR and 25G SFP28 LR.

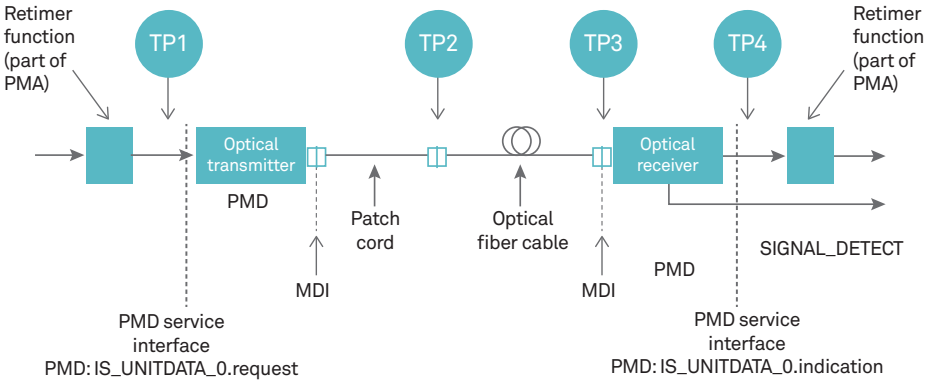
Module Type	TOSA	Driver	PD	TIA	IC
25G SFP28 LR(NRZ)	Uncooled DML TOSA	Limiting DML Driver	25G PIN	Limiting TIA	25G CDR
50G QSFP28 LR(PAM4)	Uncooled DML TOSA	Linear DML Driver	25G PIN	Linear TIA	PAM4 DSP

The main difference lies in laser drive chips, TIA chips, and data processing chips.

- Since PAM4 code has four types of level logic, the laser drive chips and TIA chips are capable of linear outputs. NRZ modules output signals in amplitude limiting mode.
- PAM4 modules use DSP to implement conversion between a 50G PAM4 signal and two 25 Gbit/s NRZ signals. NRZ modules transmit data using clock and data recovery (CDR) chips only.

3.4 PAM4-related Tests

An NRZ signal is a 2-order signal with an eye diagram of a single eye, whereas a PAM4 signal is a 4-order signal with an eye diagram of three eyes. Although PAM4 doubles the bit bearing efficiency compared with NRZ, PAM4 has noise, linearity, and sensitivity issues. This section focuses on test technologies at the physical layer.



For clarity, only one direction of transmission is shown

Figure 3-11 Diagram of 50GBASE-LR test points

IEEE defines every test point in the link model. At the physical layer, electrical signals (TP1/TP4) and optical signals (TP2/TP3) are tested. Mainstream vendors such as Tek and Keysight support physical-layer testing for PAM4.

3.4.1 Eye Diagram Test

IEEE proposes using PRBS13Q to test the PAM4 optical eye diagram. The main test indicators are eye height and width. Eye pattern parameter values of a PAM4 optical signal are defined by IEEE as follows:

- Near-end eye height = 70 mV
- Far-end eye height = 30 mV
- Near-end eye width = 0.265 UI
- Far-end eye width = 0.2 UI

Near end means that a signal is transmitted from an optical module and does not pass through a long optical fiber (TP2). Far end means that a signal passes through a long optical cable (TP3). For example, LR is a 10 km optical fiber. If a signal passes through a long optical fiber, the eye diagram quality decreases because the end-to-end insertion loss of the optical path compromises the signal quality.

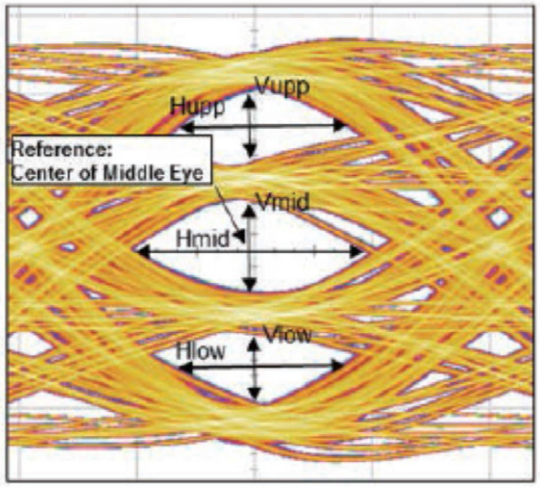


Figure 3-12 PAM4 optical eye diagram test

3.4.2 Jitter Test

Jitter tests are mainly designed for output jitters of transmitters and jitter tolerance of receivers. The test principle and scheme are the same as those for NRZ signals. IEEE will request that RJ/PJ extraction and decomposition be implemented along with the edges of PAM4 signals' 12 switching modes. The related IEEE standards are being prepared.

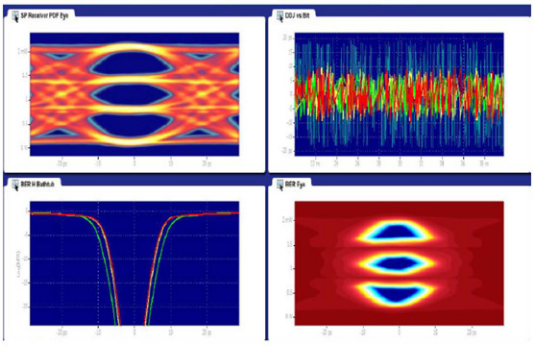


Figure 3-13 PAM4 jitter test

3.4.3 OMA Optical Power and ER Tests

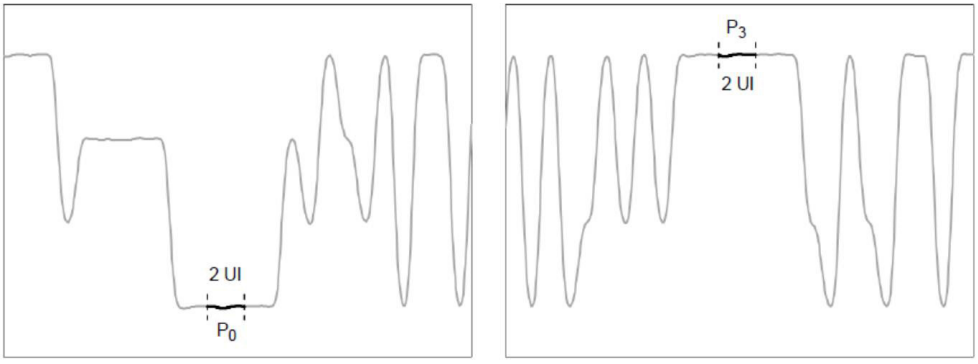


Figure 3-14 P3 and P0 defined by IEEE

ER is an important indicator to measure the performance of optical transmitters, and also the most difficult one. ER is the optical power logarithms ratio when the laser outputs the high level and low level after electric signals are modulated to optical signals. ER indicates whether a laser works at the best bias point and within the optimal modulation efficiency range. PAM4 signals have high requirements for linearity. In addition, many standards pose strict requirements on linearity. The ER test margin is limited. Therefore, implementing precise and repeatable ER tests has become a challenge now.

ER tests based on NRZ code collect statistics on high and low levels in eye diagram mode and calculate the ER logarithms ratio. In IEEE standards, ER tests based on PRBS13Q code search for the average power of the two UI time widths in the middle of seven consecutive levels 3 as the high level (P3), and search for the average power of the two UI time widths in the middle of six consecutive levels 0 as the low level (P0). Then the logarithms ratio of the two average power values is calculated, as shown in the preceding figure.

Outer Optical Modulation Amplitude (OMAouter for short) is another indicator that measures the power difference when a laser turns on and off. Therefore, OMAouter is defined as the power difference (P3 to P0) between the high level and the low level. For details about the definitions of P3 and P0, see the previous descriptions.

Both the ER and the average power can be measured by mainstream optical oscilloscopes. Tek and Keysight have launched mature optical oscilloscope products. OMA optical power is usually calculated by testing the ER and average optical power. Currently, few test instruments can directly measure the OMA optical power.

3.4.4 Forwarding Performance Tests

RFC 2544 defines the following baseline performance test indicator for networks and devices: throughput, delay, and packet loss rate. Based on network application requirements, the RFC 3393 jitter test is added to for 50G PAM4-based 50GE/200GE/400GE interfaces. Refer to the following basic configurations during a jitter test:

- Frame format: Ethernet encapsulation
- Frame length: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 1280 bytes, 1518 bytes
- Test duration: 60s
- Networking: pair, backbone, full-mesh

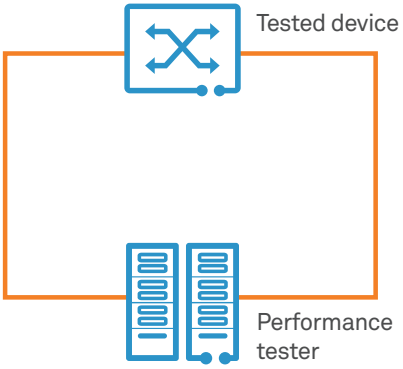


Figure 3-15 Forwarding performance test

04 Application Scenarios

4.1 Overview

50G PAM4 is the development trend of Ethernet high-speed interconnection interfaces, promotes the upgrade in the ICT industry, and applies to extensive scenarios.

4.2 5G Mobile Bearer Network

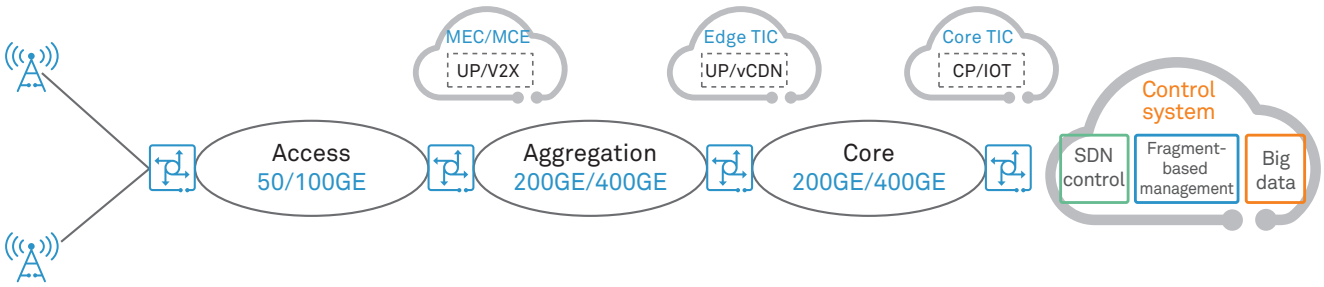


Figure 4-1 Bearer network architecture

5G can fulfill three visions: eMBB, uRLLC, and mMTC. eMBB aims to support enhanced high-bandwidth applications, including video applications such as 4K, 8K, and AR/VR. Compared with 4G, 5G improves on the spectrum efficiency by three to five times. The spectrum width of 5G starts from 100 MHz, five times that of the spectrum at the beginning of the 4G era. The bandwidth of Sub6G increases by 15 to 25 times compared with that of 4G. The high-frequency spectrum of 5G can reach over 800 MHz and the capacity also increases.

According to the bandwidth assessment method proposed by the Next Generation Mobile Networks (NGMN) Alliance, the bearer network bandwidth of 5G will evolve to 50GE/200GE at the stage of Sub6G deployment. At the high-frequency stage, the end-to-end bandwidth will evolve to 100GE/200GE/400GE.

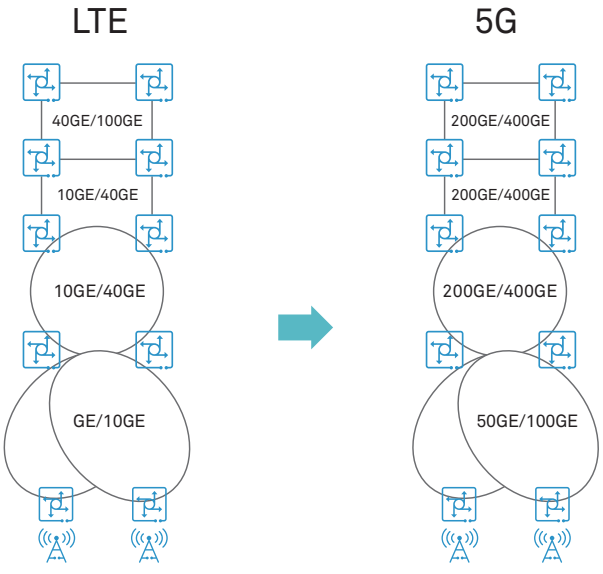


Figure 4-2 Evolution of bearer network solutions

4.3 Fixed-Line MAN

Current mainstream interfaces of fixed-line metropolitan area networks (MANs) are 10GE/40GE interfaces. With the rapid development of HD, 4K, 8K, and VA/AR, fixed-line network interfaces will soon upgrade to 50GE/200GE/400GE.

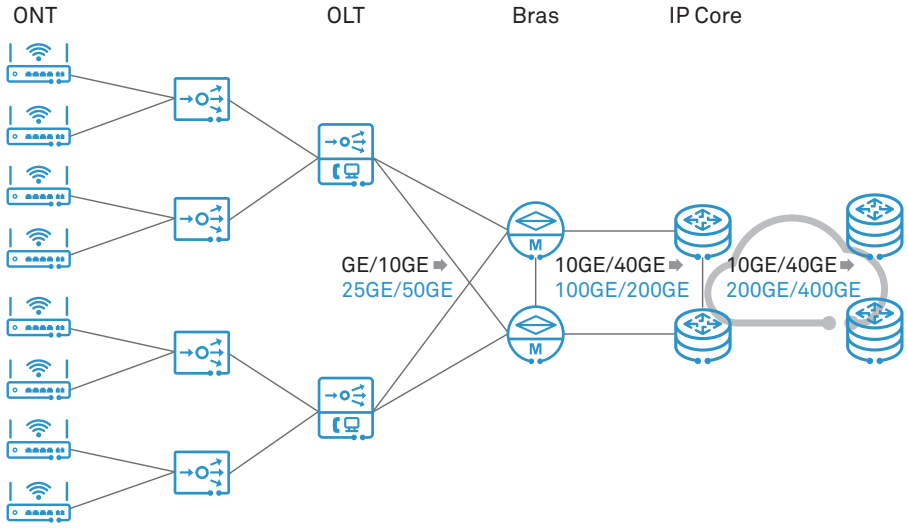


Figure 4-3 Architecture of the fixed-line MAN

4.4 DCI or DCN

Rapid development of data centers drives the upgrade of server interfaces, data center network (DCN) interfaces, and data center interconnect (DCI) interfaces from 10GE/40GE interfaces to 50GE/200GE/400GE interfaces. The 50G PAM4 industry chain constitutes a solid foundation for the fast development of data centers.

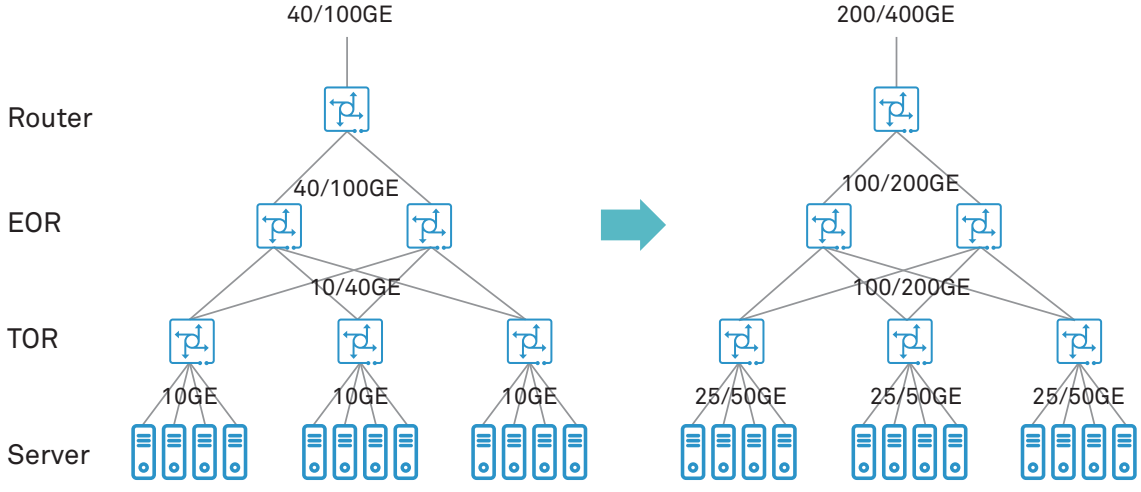


Figure 4-4 Evolution of the DCN architecture

4.5 Video Uploading in Safe City Projects

As networked, digitalized, and smart systems are becoming popular, monitoring data from security surveillance cameras grow explosively. The security assurance requirements promote the application of video surveillance technologies in various industries. Governments attach great importance to the application of big data in video surveillance, and video surveillance has gradually become a basic strategic resource of the country. By 2020, all video surveillance cameras in major public areas will be connected to the network. The number of cameras at the branch site ranges from 500 to 2000. A county-level site may contain several branch sites.

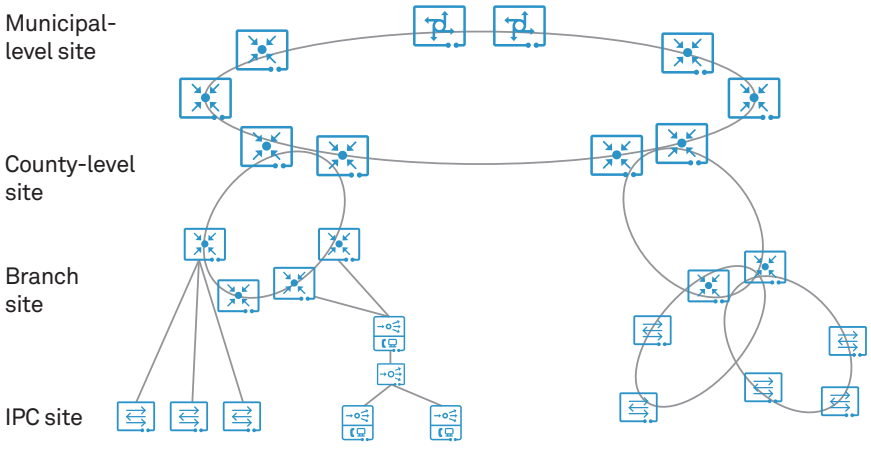


Figure 4-5 Network for video uploading

Assume that the camera bandwidth is 8 Mbit/s, the bandwidth for uploading videos from branch sites to county-level sites ranges from 10 Gbit/s to 30 Gbit/s, and that from county-level sites to municipal-level sites ranges from 20 Gbit/s to 60 Gbit/s. 50GE interfaces or above can meet requirements for uploading videos.

4.6 Uplink Server Interface

As data centers develop quickly, the network interface rate of servers in data centers has increased from 10GE to 25GE, and will reach 50GE in the future. Currently, x86 chips can support 50GE interfaces. Servers in data centers can support 50GE interfaces since a series of network controller chips that support 50GE interfaces are available on the market.

PCI Express	Line	Original	Bandwidth			
Version	Code	Transmission Rate	x1	x4	x8	x16
1	8b/10b	2.5 GT/s	2	8	16	32
2	8b/10b	5 GT/s	4	16	32	64
3	128b/130b	8 GT/s	7.87	31.50	63.01	126.03
4	128b/130b	16 GT/s	15.75	63.01	126.03	252.06

4.7 Inter-/Intra-Board Connection

High-speed SerDes interfaces are the basis of chip capacity expansion. With the encapsulation restrictions, the interface rate of a chip is directly proportional to its capacity. More and more chips support 50G PAM4 SerDes interfaces for inter- and intra-board connection, promoting the upgrade in the ICT industry. 50G PAM4 is becoming increasingly popular and platform-based and will be the basic technology in the ICT industry in the future.

05 Summary

50GE/200GE/400GE based on 50G PAM4 will surely become the basic rate of the next-generation Ethernet. As the 50G PAM4 ecosystem improves constantly, 50G PAM4 will stand out with its price-to-performance ratio and have full market potentials.

A
Acronyms and Abbreviations

200GAUI-8	200 Gb/s Attachment Unit Interface
50GAUI-2	50 Gb/s Attachment Unit Interface
AUI	Attachment Unit Interface
ASIC	Application Specific Integrated Circuit
400GAUI	400 Gb/s Attachment Unit Interface
CFP	C Form-factor Pluggable
CMOS	Complementary Metal Oxide Semiconductor
DSP	Digital Signal Processing
ER	Extinction Ratio
FEC	Forward Error Correction
IP	Internet Protocol

IEEE	Institute of Electrical and Electronics Engineer
MAC	Medium Access Control
MDI	Medium Dependent Interface
NRZ	Non-Return-to-Zero
OMA	Optical Modulation Amplitude
PAM	Pulse Amplitude Modulation
PAM4	Four-level Pulse Amplitude Modulation
PCS	Physical Coding Sub-layer
PMA	Physical Medium Attachment Sub-layer
PMD	Physical Medium Dependent Sub-layer
QSFP28	Quad Small Form-factor Pluggable 28Gbps

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